Double quantum dot with tunable coupling in an enhancement-mode silicon metal-oxide semiconductor device with lateral geometry

L. A. Tracy,[1, a)] E. P. Nordberg,[1,2] R. W. Young,[1] C. Borrás Pinilla,[3,4] H. L. Stalford,[1,3] G. A. Ten Eyck,[1] K. Eng,[1] K. D. Childs,[1] J. R. Wendt,[1] R. K. Grubbs,[1] J. Stevens,[1] M. P. Lilly,[5] M. A. Eriksson,[2] and M. S. Carroll[1]

[1)] *Sandia National Laboratories, Albuquerque, New Mexico 87185, USA*

[2)] *University of Wisconsin-Madison, Madison, Wisconsin 53706, USA*

[3)] *University of Oklahoma, Norman, Oklahoma 73019, USA*

[4)] *Universidad Industrial de Santander-Colombia, Bucaramanga, Colombia*

[5)] *Center for Integrated Nanotechnologies, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA*

(Dated: 2 November 2010)

We present transport measurements of a tunable silicon metal-oxide-semiconductor double quantum dot device with lateral geometry. Experimentally extracted gate-to-dot capacitances show that the device is largely symmetric under the gate voltages applied. Intriguingly, these gate voltages themselves are not symmetric. Comparison with numerical simulations indicates that the applied gate voltages serve to offset an intrinsic asymmetry in the physical device. We also show a transition from a large single dot to two well isolated coupled dots, where the central gate of the device is used to controllably tune the interdot coupling.

Recent progress towards demonstrating electron spin-based quantum bits in semiconductor quantum dots[1–3] has lead to renewed interest in fabrication of quantum dot structures in silicon. Silicon is a strong candidate due to a relatively small electronic spin-orbit coupling, low concentration of nuclear spins (a potential source of electron spin decoherence), and the ability to leverage mature silicon fabrication technologies.

We report low-temperature transport measurements of a Si metal-oxide semiconductor (MOS) double quantum dot (DQD). In contrast to previously reported measurements of DQD's in Si MOS structures[4–9], our device has a lateral gate geometry very similar to that used by Petta *et al.*[2] to demonstrate coherent manipulation of single electron spins. This gate design[10] provides a high degree of tunability, allowing for independent control over individual dot occupation and tunnel barriers, as well as the ability to use nearby constrictions to sense dot charge occupation[11].

Figure 1(a) shows a top-down scanning electron microscope (SEM) image of the partially processed device and a schematic of the final device cross section. The upper Al top gate is used to accumulate carriers at the Si-SiO_2 interface. The lower, patterned polycrystalline silicon (polysilicon) gates are used to deplete carriers to define the DQD region. The device is fabricated on a lightly p-type Si substrate (2 - 20 Ω cm). Initial fabrication steps (Ohmic contact formation to channel, gate oxide growth, and polysilicon deposition and doping) are performed in a fully qualified CMOS facility. Ohmic contacts (not shown in Fig. 1(a)) are formed by implantation of As, followed by a 900 °C, 15 min. activation anneal. Next, a 35 nm SiO_2 gate oxide is grown in dry O_2 at 900°C, with a subsequent N_2 anneal at 900°C for 30 min., immediately followed by polysilicon deposition (200 nm) and doping. The lower-level polysilicon depletion gates are defined by e-beam lithography and dry etch and are 200 nm tall with a ∼100 nm linewidth for the narrowest features (see Fig. 1(a)). After the polysilicon etch, the device is exposed to a thermal oxidation step which forms a 30 nm layer of SiO_2 on the surface of the polysilicon gates. Finally, the polysilicon is further isolated from the global Al top gate by 60 nm of Al_2O_3 formed via atomic layer deposition (ALD). More details about the fabrication of this device and its operation in single-dot mode can be found in Ref. 12.

The device conductance is experimentally determined via standard low-frequency lock-in measurements with an rms ac source-drain bias of 10 - 50 μV. Unless otherwise noted, the Al top gate TG, T, L, and R (see Fig 1(a)) voltages are held constant at V_{TG} = 5 V, V_T = -0.3 V, V_L = 0 V, and V_R = -2 V. All measurements shown are performed in a dilution refrigerator with a temperature of $T \sim 20$ mK. We note that although the conductance of the device continues to evolve below a fridge temperature of 100 mK, we cannot be certain our dot electron temperature is equal to our fridge temperature in this regime. However, the precise value of the electron temperature should not affect the conclusions of this letter.

Figures 1(b)-(e) show DQD conductance versus left and right plunger gate voltages V_{LP} and V_{RP} at four different center plunger voltages V_{CP}, demonstrating the ability to tune the DQD from a highly-coupled regime, where the transport is reminiscent of that expected for a large, single dot, to a weakly-coupled regime, where conduction can only take place at the so-called triple points. As expected, the interdot coupling shows a strong dependence on V_{CP}, whereas we find a nearly negligible dependence on V_{LP} and V_{RP}.

In Fig. 2(a) we show DQD conductance versus V_{LP} and V_{RP} at V_{CP} = -1.2 V. The capacitance between the plunger gates and dots can be extracted from the dimensions shown in Fig. 2(a): $C_{LP-LD} = e/\delta V_{LP-LD} = 8.1$

[a)] Electronic mail: latracy@sandia.gov

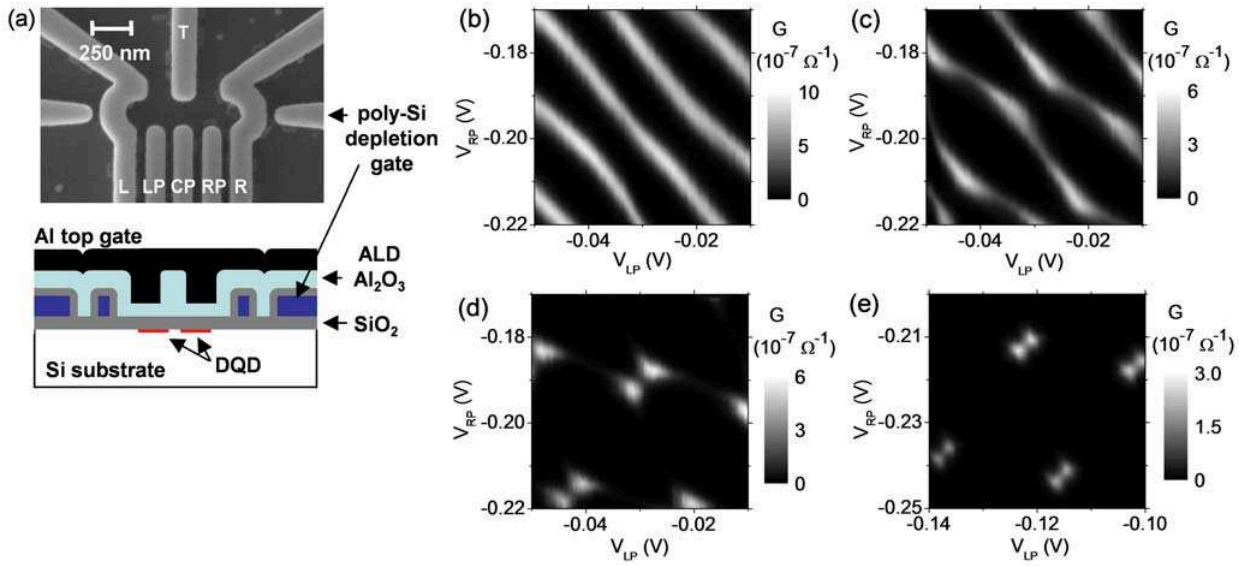

FIG. 1. (a) SEM image of partially processed device showing polysilicon gates and schematic of final device cross-section. (b) - (e) Conductance of double dot G versus $V_{\rm LP}$ and $V_{\rm RP}$, showing transition from a large single-dot to a well-defined double dot, at CP gate voltages (b) $V_{\rm CP}$ = -0.6 V, (c) $V_{\rm CP}$ = -0.8 V, (d) $V_{\rm CP}$ = -1.0 V, (e) $V_{\rm CP}$ = -1.2 V, for $V_{\rm T}$ = -0.3 V, $V_{\rm L}$ = 0 V, and $V_{\rm R}$ = -2 V.

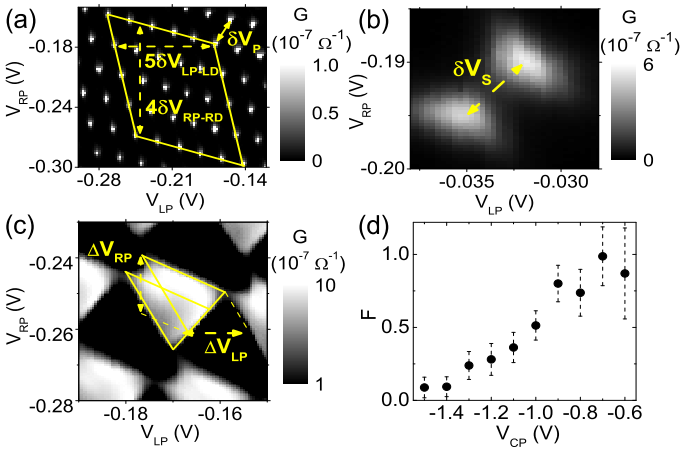

FIG. 2. (a) DQD conductance G vs. $V_{\rm LP}$ and $V_{\rm RP}$ at $V_{\rm CP}$ = -1.2 V, showing LP (RP) voltage required to change the occupation of the left dot (right dot) by 5 (4) electrons: $5\delta V_{\rm LP-LD}$ ($4\delta V_{\rm RP-RD}$). (b) Closer view of triple points at $V_{\rm CP}$ = -1.2 V for zero dc source drain bias. (c) Triple points at $V_{\rm CP}$ = -1.2 V for dc source-drain bias $V_{\rm sd}$ = 0.5 mV, showing dimensions of bias triangles. (d) Interdot coupling F versus $V_{\rm CP}$ determined from plunger gate voltage separation of triple points.

aF, $C_{\rm RP-RD} = e/\delta V_{\rm RP-RD}$ = 5.3 aF. Figure 2(c) shows bias triangles at a finite dc source-drain bias of 0.5 mV at $V_{\rm CP}$ = -1.2 V. Using $C_{\rm LP-LD(RP-RD)}/C_{\rm LD(RD)} = V_{\rm sd}/\Delta V_{\rm LP(RP)}$ we find total dot capacitances $C_{\rm LD}$ = 210 aF and $C_{\rm RD}$ = 170 aF[13].

Figure 2(b) shows a closer view of single pair of triple points at $V_{\rm CP}$ = -1.2 V and zero dc source-drain bias. The distance between triple points in plunger gate voltage space $\delta V_{\rm S}$, as shown in Fig. 2(b), can be used to estimate the interdot coupling. In Fig. 2(d) we show the fractional splitting of the triple point F versus CP gate voltage, where $F \equiv 2\delta V_{\rm S}/\delta V_{\rm P}$ (see Fig. 2(a), (b)) is a measure of the interdot coupling, defined as the ratio of the diagonal separation between triple points to the separation between charge domains[14,15]. The error bars are determined by the ability to visually resolve the position of the triple points on a honeycomb plot. Figure 2(d) shows that sweeping CP smoothly varies F from nearly zero to one, demonstrating the ability to tune the DQD from weakly-coupled to a regime where the dots are fully merged[14,16].

Figure 3(a) shows a comparison between experimentally determined capacitances from the various gates to the dots and values determined via modeling. The values $C_{\rm MEAS}$ in Fig. 3(a) are obtained from honeycomb plot dimensions from double dot transport, or from the gate voltage period of Coulomb blockade oscillations in single dot transport. For double dot transport, the gate voltages are $V_{\rm TG}$ = 5 V, $V_{\rm T}$ = -0.3 V, $V_{\rm L}$ = 0 V, $V_{\rm LP}$ = 0 V, $V_{\rm CP}$ = -1.2 V, $V_{\rm RP}$ = 0 V, $V_{\rm R}$ = -2 V. Values marked with an asterisk indicate capacitances from single dot transport, obtained for the left dot by setting $V_{\rm R}$ = +1 V, or for the right dot by using $V_{\rm L}$ = +1 V, while maintaining all other gate voltages the same as used for double dot transport. Error bars are determined by variations in the charge transition period.

Figure 3(b) shows a contour plot of calculated electron density in the DQD region at gate voltages equal to those used for the experimental capacitances. The calculations are semiclassical (Thomas-Fermi approximation) and were performed using TCAD Sentaurus[17], a

(a)

gate – dot	C_{MEAS} (aF)	$C_{Sentaurus}$ (aF)	$C_{CFD\text{-}ACE}$ (aF)
RP - RD	5.3 ± 0.1	3.3	5.3
RP - LD	1.8 ± 0.1	1.6	1.6
LP - LD	8.1 ± 0.1	9.4	8.1
LP - RD	1.6 ± 0.1	0.7	1.2
R - RD	11.6 ± 0.1	4.6	11.5
L - LD	17.3 ± 0.1	34.4	17.3
T – RD	7 ± 1*	8.8*	7.1
T – LD	8 ± 1*	9.2*	8.1
CP – RD	5 ± 2*	5.3*	4.9
CP – LD	6 ± 1*	6.1*	5.9
TG – RD	21 ± 5*	12.9*	18.9
TG – LD	23 ± 2*	14.5*	22.4

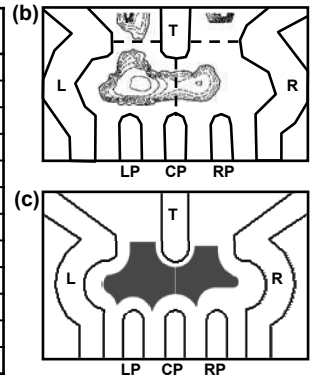

FIG. 3. (a) Table of capacitances between dots (right dot (RD) and left dot (LD)) and gates (as labeled in Fig. 1(a), comparing measured and calculated values. $C_{\rm MEAS}$ are experimental values for the case $V_{\rm CP}$ = -1.2 V, $C_{\rm Sentaurus}$ values are computed using a semiclassical model for dot electron density, and $C_{\rm CFD-ACE}$ values are calculated by treating the dots as metallic regions defined by the shaded areas sketched in (b). Asterisks indicate capacitances from single-dot transport, obtained by setting $V_{\rm R}$ ($V_{\rm L}$)= +1 V for left (right) dot measurement. (b) Calculated electron density in dot regions relative to polysilicon gates, where the dotted lines are contours of electron density from 1 to 7×10^{11} cm^{-2} in 1×10^{11} cm^{-2} increments. The dashed lines define the boundary between the left and right dot regions and between the dot regions and the leads. (c) Sketch of dot region used to obtain good agreement between experimental and calculated capacitances. Shaded area represents dot region, which is treated as a metallic (perfect conductor) region in order to calculate capacitances.

commercial device simulation package. The capacitances $C_{\rm Sentaurus}$ are obtained by integrating the charge density over the entire left or right dot region and calculating the change in the integrated dot charge due to a small change in gate voltage. The boundaries used to separate the left dot from the right dot and the dot region from the leads are shown by the dashed lines in Fig. 3(b).

In Fig. 3(c), we show a model dot region (shaded area) used to calculate capacitances between the various gates and dots by treating the dot region as a perfectly-conducting metallic sheet. These capacitance calculations were performed using CFD-ACE+[18], a finite-element modeling package. The shape of the dot was chosen by starting with a region which approximately follows the contours defined by the gates, and then modifying the distance between the dot and various gates as to obtain good agreement with the experimental capacitances $C_{\rm MEAS}$ listed in Fig. 3(a).

The agreement between the capacitances predicted by the Sentaurus calculation and those obtained from experiment is relatively poor. As shown in Fig. 3(b), the Sentaurus calculation predicts an asymmetric dot region, resulting in a capacitance of $C_{\rm R-RD}$ = 4.6 aF from the R gate to right dot, versus $C_{\rm L-LD}$ = 34.4 aF from the L gate to left dot. This extreme asymmetry does not reflect transport in the actual device, which yields $C_{\rm R-RD}$ = 11.6 aF versus $C_{\rm L-LD}$ = 17.3 aF. The dot regions shown in Fig. 3(c), which result in reasonable agreement between $C_{\rm MEAS}$ and $C_{\rm CFD-ACE}$, predict a right dot that is smaller than the left dot, but not as dramatically so as suggested by the contours in Fig. 3(b).

The disagreement between $C_{\rm MEAS}$ and $C_{\rm Sentaurus}$ suggests that the Sentaurus calculation fails to capture some aspect of the actual device, such as unintentional imperfections that may be present in the experiment, but are not included in the calculation. For example, a spatially varying distribution of charge in the dielectric regions or variations in film thickness (e.g. non-uniform Al_2O_3 deposition) can lead to unintentional variations in electron density in the dot region. However, the relative symmetry of the dot contours shown in Fig. 3(c) (as compared to Fig. 3(b)) suggests that by use of asymmetric gate voltages ($V_{\rm R}$ = −2 V versus $V_{\rm L}$ = 0 V) we are able to partially compensate for this disorder.

In conclusion, we have demonstrated a gate-defined Si MOS double quantum dot with lateral geometry. Comparison between experimental and calculated capacitances suggest the presence of disorder and that we are able to partially compensate for this disorder by adjustment of gate voltages, due to the tunability of our lateral geometry. Our data also shows the ability to control the interdot coupling over a wide range of energies. Similar device structures may allow for further study of DQDs in the few electron regime, which would be of interest for quantum computing applications.

ACKNOWLEDGMENTS

This work was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences user facility, and was supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multi-program laboratory operated by Sandia Corporation, a wholly owned subsidiary Lockheed-Martin Company, for the U. S. Department of Energy's National Nuclear Security Administration under Contract No. DE-AC04-94AL85000.

[1] D. Loss and D. P. DiVincenzo, Phys. Rev. A **57**, 120 (1998).
[2] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, A. C. Gossard, Science **309**, 2180 (2005).
[3] F. H. L. Koppens, C. Buizert, K. J. Tielrooij, I. T. Vink, K. C. Nowack, T. Meunier, L. P. Kouwenhoven, and L. M. K. Vandersypen, Nature **442**, 766 (2006).
[4] L. P. Rokhinson, L. J. Guo, S. Y. Chou, and D. C. Tsui, Phys. Rev. B **63**, 035321 (2001).
[5] A. Fujiwara, H. Inokawa, K. Yamakazi, H. Namatsu, Y. Takahashi, N. M. Zimmerman, and S. B. Martin, Appl. Phys. Lett. **88**, 053121 (2006).
[6] S. J. Shin, J. J. Lee, R. S. Chung, M. S. Kim, E. S. Park, J. B Choi, N. S. Kim, K. H. Park, S. D. Lee, N. Kim, and J. H. Kim, Appl. Phys. Lett. **91**, 043114 (2007).
[7] H. Liu, T. Fujisawa, H. Inokawa, Y. Ono, A. Fujiwara, and Y. Hirayama, Appl. Phys. Lett. **92**, 222104 (2008).

[8] W. H. Lim, H. Huebl, L. H. Willems van Beveren, S. Rubanov, P. G. Spizzirri, S. J. Angus, R. G. Clark, and A. S. Dzurak, Appl. Phys. Lett. **94**, 173502 (2009).
[9] B. Hu and C. H. Yang, Phys. Rev. B **80**, 075310 (2009).
[10] M. Ciorga, A. S. Sachrajda, P. Hawrylak, C. Gould, P. Zwadzki, S. Jullian, Y. Feng, and Z. Wasilewski, Phys. Rev. B **61**, R16315 (2000).
[11] E. P. Nordberg, H. L. Stalford, R. Young, G. A. Ten Eyck, K. Eng, L. A. Tracy, K. D. Childs, J. R. Wendt, R. K. Grubbs, J. Stevens, M. P. Lilly, M. A. Eriksson, and M. S. Carroll, Appl. Phys. Lett. **95**, 202102 (2009).
[12] E. P. Nordberg, G. A. Ten Eyck, H. L. Stalford, R. P. Muller, R. W. Young, K. Eng, L. A. Tracy, K. D. Childs, J. R. Wendt, R. K. Grubbs, J. Stevens, M. P. Lilly, M. A. Eriksson, and M. S. Carroll, Phys. Rev. B **80**, 115331 (2009).
[13] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, Rev. Mod. Phys. **75**, 1 (2003).
[14] C. Livermore, C. H. Crouch, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Science **274**, 1332 (1996).
[15] J. M. Golden and B. I. Halperin, Phys. Rev. B **53**, 3893 (1996).
[16] C. B. Simmons, Madhu Thalakulam, B. M. Rosemeyer, B. J. Van Bael, E. K. Sackmann, D. E. Savage, M. G. Lagally, R. Joynt, Mark Friesen, S. N. Coppersmith, and M. A. Eriksson, Nano Lett. **9**, 3234 (2009).
[17] Synopsys, Inc., Mountain View, California, USA, 2009.
[18] ESI Group, Paris, France, 2008.